A very warm welcome to the 7th joint EuroSOI – ULIS 2021 Conference

September 1-3, 2021 - Caen, Normandy, France

This Conference aims at gathering together in an interactive forum all scientists and engineers working in the field of SOI technology and advanced nanoscale devices.

One of the key objectives of the conference is to promote collaboration and partnership between different academia, research and industry players in the field.

After a virtual 2020 edition, if sanitary condition will permit, the 2021 EUROSOI-ULIS event will held as in-person Conference hosted by the Normandy University (ENSICAEN, UNICAEN, ESIGELEC) in Caen, inside the William the Conqueror Castel, in the auditorium of Museum of Fine Arts.

The organizing committee invites scientists and engineers working on SOI technology and advanced nanoscale devices to actively participate by submitting high quality, original contributions.

Original 2-page abstracts with illustrations will be accepted for review in pdf format.

The authors of the **accepted contributions** will be requested to provide a **4-page extended abstract** which will be included in the **conference proceedings** (with IEEE technical sponsorship and ISBN index) and in the **IEEE Xplore® digital library**.

Outstanding papers will be **invited for publication** in a special issue of **Solid-State Electronics**.

A best paper award, renamed "The Androula Nassiopoulou Best Paper Award" in tribute to her, will be attributed by the **SINANO institute**.

A best poster award will be attributed by **ELSEVIER.**

Important dates :

abstract submission deadline : Mai 17, 2021

notification of acceptance : June 4, 2021

final paper submission: June 28, 2021

Papers in the following areas are solicited:

- Advanced SOI materials and structures; physical mechanisms and innovative SOI-like devices.
- New channel materials for CMOS: strained Si, strained SOI, SiGe, GeOI, III-V and high mobility materials on insulator; carbon nanotubes; graphene and other two-dimensional materials.
- Properties of ultra-thin films and buried oxides, defects, interface quality; thin gate dielectrics: high-κ materials for switches and memory.
- Nanometer scale devices: technology, characterization techniques and evaluation metrics for high performance, low power, reliability, high frequency and memory applications.
- Alternative transistor architectures including FDSOI, Nanowire, FinFET, MuGFET, vertical MOSFET, FeFET and Tunnel FET, MEMS/NEMS, Beyond-CMOS nanoelectronic devices.
- New functionalities in silicon-compatible nanostructures and innovative devices representing the More than Moore domain, nanoelectronic sensors, biosensor devices, energy harvesting devices, RF devices, imagers, etc.
- CMOS scaling perspectives; device/circuit level performance evaluation; switches and memory scaling; three-dimensional integration of devices and circuits, heterogeneous integration.
- Transport phenomena, compact modeling, device simulation, front- and back-end process simulation.
- Advanced test structures and characterization techniques, parameter extraction, reliability and variability assessment techniques for new materials and novel devices.

Confirmed Plenary Talks Speakers:

- Alexander Zaslavsky (Brown University, USA)
- Anne Vandooren (imec, Belgium)
- Frédéric Allibert (SOITEC, France)
- Jean-Michel Sallèse (EPFL, Switzerland)
- Sorin Cristoloveanu (IMEP Minatec, Grenoble, France)
- Sorin Voinigescu (University of Toronto, Canada)

Instutitional partners: